Block inverters for the CR UA0007C1

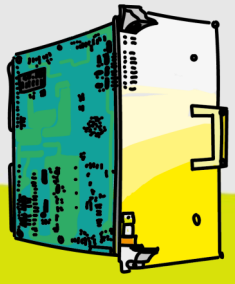
Safe and reliable automation

Inverter block for drive control UA0007C1 of Control System SandRA Z100 line

The **UA0007C1** block is part of the robust and powerful **SandRA Z100** series of process stations, whose safety and reliability features make it the ideal solution for use in the nuclear power industry. **ZAT** has been continuously active in this field since **1972** and continues to bring new innovative solutions.

The drive control inverter block is used to supply and control linear stepper motor of the control mechanism drive of the **VVER1200**. All binary inputs and outputs are **galvanically isolated** from the internal circuits of the block. Input and output data are transmitted to other parts of the system via **SSIO3** communication. The block is equipped with a diagnostic system that monitors the status of the block and other functions. Status and user variables are then indicated by **LEsD** on the front panel.

- **Designed for 19” rack.**
- **Board dimensions 142 x 266 x 388 mm**
- **Data transfer via SSIO3 communication**
- **4 binary inputs of free contact type**
- **6 binary outputs**
- **9 special pulse binary inputs.**
- **6 special pulse binary outputs.**
- **The design and circuit design enables the Hot Swap function**

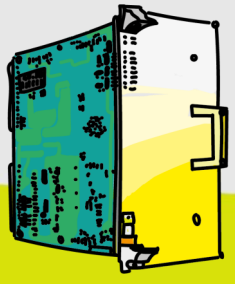


Mechanical parameters and weight

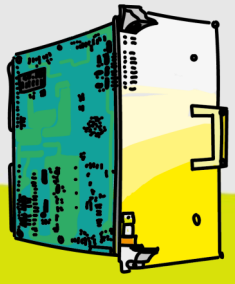
Parameter	Conditions	Min.	Type	Max.	Units
Block dimensions			142 x 262 x 328		mm
Front panel dimensions			142 x 262		mm
Weight			4.85		kg

Electrical parameters

Parameter	Conditions	Min.	Type	Max.	Units
Power supply					
Power voltage (DC)	U_{nap}	19.2	48	60	V
Consumption	U_{nap} = 48V		260	320	mA
Power supply of the power section					
Power voltage - phase I (AC)	3 phase	140	175	210	V
Consumption			4	10	A
Power outputs					
Number	(independently)		3		
Output voltage		0		200	V
Output current[2]			7.5	20	A
Modulation frequency[3]		0.5		30	kHz
Temperature sensor					
Number [4]			3		
Measuring range		-55		+125	°C
Measuring accuracy			±2		°C
Binary inputs 24V (internally powered)					
Number of inputs	With a common positi-veinternal power supply		4		
Logical levels for positive polarity [5] log. H log. L	Given by a common positive power supply. The input is activated by connecting to ground		 240	 30	 V V



Parameter	Conditions	Min.	Type	Max.	Units
Input current consumption	U_{in}=24V		9	12	mA
Surge filtering time constant [6]			1		ms
Insulation strength input / internal circuit board		2000			V DC
Binary outputs (two-way, "free contact" type)					
Number of outputs	5 NO + 1 NC		6		
Load voltage	peek AC			170	V
Current load of outputs				100	mA
Resistance in NC	I = 100 mA		23	35	Ω
Insulation strength output / internal circuit board		2000			V DC
Insulation strength output/output		700			V DC
Special pulse binary inputs.					
Number of inputs			9		
Input voltage			5	10	V
Input current consumption	U_{in}=5V		5	6.5	mA
Input frequency		1		20	kHz
Insulation strength output/internal board circuits		2000			V DC
Special pulse binary outputs.					
Number of outputs			6		
Output voltage			5		V
Current load of outputs				8	mA
Modulation frequency			10		kHz
Insulation strength output/internal board circuits		2000			V DC



Parameter	Conditions	Min.	Type	Max.	Units
Number of communication lines			3		
Baud rate				8	Mbps
Communication type			slave		
Insulation strength of SSIO3 line LVDS / internal circuit board		2000			V DC
USB interface (service channel)					
Number of communication channels			1		
Baud rate			12		Mbps
Insulation strength of USB / internal circuit board		700			V DC

[2] *The value and sequence of the output current for individual operating modes is set from the ASW of the inverter.*
[3] *The modulation frequency depends on the load impedance and the set parameters of the controller.*
[4] *One temperature sensor is on the MK0084M1 module, the second on the the third on the MK0088A1 and the fourth on the IGBT module cooler (MK0088A1).*
[5] *The logic levels of the binary inputs are set internally.*
[6] *According to FW– the time constant is realized during signal processing in FPGA.*

This document contains the product UA0007C1 and follows the"Z100 Technical conditions" No. C4-2443 constituting its integral part.